REMARKS

Prior to the present Amendment, claims 1-14 were all the claims pending in the application. Claims 1-14 stand rejected on prior art grounds. By the present Amendment, Applicant has canceled claims 6 and 7 without prejudice or disclaimer. Thus, upon entry of the present Amendment, claims 1-5 and 8-14 will be all the claims pending in the application.

I. Claim Rejections - 35 U.S.C. § 102

Claims 1-4, 8-14 stand rejected under 35 U.S.C. 102(e) as allegedly being anticipated by U.S. Patent Appl. Publ. No. 2004/0061671 to Kawasaki et al. ("Kawasaki"). Applicant respectfully traverses the rejection as follows.

A. Claim 1

Amended claim 1 recites, *inter alia*:

> A display apparatus with an active matrix display panel having a plurality of pixel sections each including a light emitting element and two equivalent driving circuits which each have a thin film transistor, said display apparatus comprising:...
>
> supplying a scanning pulse to each pixel section in the one row, and generating a data pulse corresponding to a first gate voltage of said thin film transistor for light emission driving of the light emitting element in the at least one pixel section and a reset pulse to the at least one pixel section when supplying the scanning pulse, the reset pulse corresponding to a second gate voltage of said thin film transistor for making a gate-to-source voltage of said thin film transistor a voltage having opposite polarity to that of a voltage obtained during the light emission driving, or zero voltage, wherein
>
> each of the two driving circuits applies the first gate voltage corresponding to the data pulse to a gate of said thin film transistor in response to said scanning pulse in a display mode period, and applies the second gate voltage corresponding to the reset pulse to the gate of said thin film transistor in response to said scanning pulse in a reset mode period, and

> the two driving circuits are assigned with different mode periods by alternately switching between the display mode period and the reset mode period for each frame.

Kawasaki teaches a display apparatus in which a predetermined cycle is formed by a pixel turn-on time period T1 and a threshold value control time period T2. *See* Kawasaki at paragraph [0073]; Fig. 1. As shown in Fig. 1 of Kawasaki, a signal voltage Vs as luminance information is taken from a signal line during the pixel turn-on time period T1, and a threshold value control voltage Vr having opposite polarity to that of the luminance information is taken from the signal line during the threshold value control time period T2. *See* Kawasaki at paragraph [0073].

Kawasaki fails to teach or suggest that each pixel section includes two equivalent driving circuits. In rejecting claim 6, the subject matter of which has been incorporated into claim 6, the Examiner relies on Figs. 11 and 12 of Kawasaki as allegedly teaching that a pixel section comprises two equivalent driving circuits each having a thin film transistor. *See* Office Action at page 7. However, in Figs. 11 and 12 of Kawasaki, only one driving circuit including Trl - Tr3, 201, and C1 is provided for each pixel. Therefore, Kawasaki fails to teach or suggest "a plurality of pixel sections each including a light emitting element and two equivalent driving circuits which each have a thin film transistor."

Further, Kawasaki fails to teach or suggest that two driving circuits are assigned with different mode periods by alternately switching between the pixel turn-on time period T1 and the threshold value control time period T2.

In rejecting claim 6, which is presently incorporated into claim 1, the Examiner relied in part upon U.S. Patent No. 5,748, 165 to Kubota et al. ("Kubota"). However, Kubota merely teaches an image display device having one data signal line SLm in every pixel column, and one

scanning signal line GLn in every pixel row, as shown in Figs. 16 and 17. *See* Kubota at col. 20, lines 40-43. In the data signal line SLm, alternately, positive polarity data and negative polarity data are written, and data are supplied into the data signal lines SLm from two data line driving circuits SD1 and SD2 differing in the operating power supply level, and changeover of power supply levels VCC1/VEE1 and VCC2/VEE2 of data signal line SLm in every field period is done by changing over the operating power supply level of the two data line driving circuits SD1 and SD2. *See* Kubota at Fig. 16; col. 20, lines 43-51. In Fig. 17, the changeover of power supply level VCC1/VEE1 and VCC2/VEE2 of the data signal line in every field period is effected by a switching circuit SEL which utilizes vertical synchronous signal of image data or the like and which is installed between the data signal line Slim and two data line driving circuits SD1 and SD2. *See* Kubota at Fig. 17; col. 20, lines 60-67.

However, Kubota does not teach or suggest a pixel section having two equivalent driving circuits for each pixel. Kubota merely discloses that each pixel section has only a switching element SW and pixel capacitance Cl, as shown in Figs 16 and 17. Therefore, Applicant submits that Kubota fails to cure the deficient teachings of Kawasaki with respect to claim 1.

Accordingly, Applicant submits that claim 1 is patentable over Kawasaki and Kubota because the references fails to teach or suggest all of the features of claim 1.

B. Claims 2-4 and 8-14

Since claim 11 recites features similar to those set forth above in conjunction with claim 1, Applicant submits that claim 11 is patentable over Kawasaki for at least reasons similar to those set forth for claim 1. Since claims 2-4 and 8-10 are dependent upon claim 1, and claims 12-14 are dependent upon claim 11, Applicant submits that 2-4, 8-10, and 12-14 are patentable at least by virtue of their respective dependencies.

II. Claim Rejections Under 35 U.S.C. § 103(a) over Kawasaki in view of Kubota

Claims 5 and 6 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Kawasaki in view of Kubota.

Since claim 5 is dependent upon claim 1, and Kubota fails to cure the deficient teachings of Kawasaki with respect to claim 1, Applicant submits that claim 5 is patentable at least by virtue of its dependency. Since claim 6 has been canceled without prejudice or disclaimer, Applicant submits that the rejection of claim 6 is now moot.

III. Claim Rejection Under 35 U.S.C. § 103(a) over Kawasaki in view of U.S. Patent Appl. Publ. No. 2003/0025656 to Kimura ("Kimura")

Claim 7 stands rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Kawasaki in view of Kimura. Since claim 7 has been canceled without prejudice or disclaimer, Applicant submits that the rejection of claim 7 is now moot.

IV. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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